NXP
TIME SENSITIVE NETWORK SOLUTIONS

EMBEDDED COMPUTING CONFERENCE 2017

ROGER UNGERER
PRINCIPAL FAE

5, SEPT., 2017
DIGITAL NETWORKS
INDUSTRIAL - SOLUTIONS
Industry 4.0 Requires Scalable Application Processing

Improving time to market, manufacturing flexibility, and increasing quality and efficiency will require smarter, connected businesses

Powering Industrial Applications for over 6 decades  1 Billion Industrial Application Processors Shipped

<table>
<thead>
<tr>
<th>Legacy</th>
<th>Longevity</th>
<th>Extreme Op</th>
<th>Security</th>
</tr>
</thead>
</table>

Complete Solutions for Industrial Processing
Real time response to IoT data

Deterministic Ethernet for Operational Technology Traffic

Increasing security threats and costs

Analytics Driving Edge Computing

Network Convergence

Secure Platform

IoT data requires local processing to make immediate decisions and reduce the data passed on to the cloud.

One network to support both IT and OT data. TSN guarantees bandwidth, latency, and reliability for OT streams.

The IoT increases the number of targets for cyber attacks, and now devices can interact with the physical world.
TSN STANDARD
TSN IEEE Standardization Overview

Time Sync:
Timing and Sync 802.1AS includes a profile of IEEE 1588

Bounded Low Latency:
Credit Based Shaper 802.1Qav
Preemption 802.3br & 802.1Qbu
Scheduled Traffic 802.1Qbv
Cyclic Q-ing & Forward 802.1Qch
Async Shaping P802.1Qcr

TSN Components
- Synchronisation
- Reliability
- Latency
- Resource Management

Ultra Reliability:
P802.1CB Frame Replication and Elimination
802.1Qca Path Control
802.1Qci Per-Stream Filtering
P802.1AS-Rev Time sync

Dedicated Resources and API:
802.1Qat Stream Resolve Protocol
P802.1Qcc TSN configuration
P802.1Qcp YANG
P802.1CS Link-local Resolve Protocol

Zero congestion loss

Guaranteed data transport with bounded low latency, low delay variation, and extremely low loss

Source: János Farkas - Introduction to IEEE 802.1, May 2017
Deterministic Ethernet at Gigabit Speed Rate

**Time Sensitive Networking (TSN)**

- Extend use cases from audio/video applications to control systems
- Reduced worst-case delays
  - 4 μs or less per hop @ 1 Gbps for short messages (plus cable delays)
- Improved robustness:
  - Alternative paths with “instant” switchover
  - Seamless redundancy using multiple simultaneous streams
  - Multiple clock sources with “instant” switchover
- Scalability
  - Reduced management traffic for reservations and configuration

IEEE802.1 TSN Task Group

2017 Market
40 mio ports/yr
11% CAGR
INDUSTRIAL TSN USE CASES
Industrial Products

Programmable Logic Controller (PLC)
Gateway between TSN and previous generation industrial Ethernet protocol
TSN to endpoints
Key attributes: TSN, TSN Bridge to Industrial Ethernet Master

Industrial Control and Instrumentation
Key attributes: ARMv8, TSN
Industrial Control Solutions

1st Target for TSN Deployments
- Converged IT and OT networks
- Allow deterministic control to control domains using existing industrial protocols
2\textsuperscript{nd} Wave for TSN Deployments

- TSN deployed into new field domain applications
TSN SOLUTIONS
Leading the 64-bit ARM and Multicore Innovation

Remote Terminal, PLC, Industrial Networks, Low Power Nodes

Industrial Firewall, Managed Switches, Gateways, Access Points, FPGA Host MPU

Access Gateway, WLAN, Intelligent Edge, vCPE, High End Industrial Drives

Low Power Nodes

SDN, NFV, Cloud Networking, Storage

A72

A7

A53

A72

A72

A53

A72

A72

A72

A53

A72

A72

A72

A72

A72

A72

A53

A72

LS1012A
- Single Core
- 800 MHz
- 2 Gb/s Packet
- 1 Gb/s Crypto
- 1-2 Watt
- Lowest Power 64-bit ARM

LS1021A
- 2 Cores
- 1 GHz
- 2 Gb/s Packet
- 1 Gb/s Crypto
- 2 Watt
- CAN

LS1028A
- 2 Cores
- 1.3 GHz
- 5 Gb/s Packet
- 5 Gb/s Crypto
- 4-9 Watt
- GPU
- 1st with TSN switch

LA1575A
- 2/4 Cores
- 10+ Gb/s Packet
- Wireless Radio
- 802.11 ac/ax
- Pre 5G
- Expl. 802.11 ad

LS1043A
- 4 Cores
- DPAA1 accelerator
- 20 Gb/s Packet
- 10 Gb/s Crypto
- 6-12 Watt
- 1st 64-bit ARM MPU for gateways and access points

LS1046A
- 4 Cores
- DPAA2 accelerator
- 20 Gb/s Packet
- 10 Gb/s Crypto
- 15-20 Watt
- 1st 8 x A53 ARM
Next generation programmable offload

LS1088A
- 4/8 Cores
- DPAA2 accelerator
- 40 Gb/s Packet
- 20 Gb/s Crypto
- 20-35 Watt
- 1st 8 x A82 ARM
Next generation programmable offload

LA1575A
- 2/4 Cores
- 10+ Gb/s Packet
- 5 Gb/s Crypto
- 3.5-8 Watt
- 1st 64-bit ARM MPU for gateways and access points

www.nxp.com/layerscape
Allows developers to design with the new IEEE Time-Sensitive Networking (TSN) standard

• provided with the OpenIL industrial Linux® distribution
  – support for netconf configuration of the TSN features
  – real-time performance with Xenomai.

• Complete design files for the board, as well as detailed bill of materials (BOM) at no additional charge available.

• Orderable Part Number: LS1021ATSN-PA
  Link: TSN Reference Design
LS1021 + SJA1105T TSN Reference Design

LS1021A

1 Gbps

SJA1105T

TSN
1 Gbps Switch Port

Gb Ethernet
TSN Demo

• Overview
  ▪ 3 host Linux machines connected through a switch
  ▪ 2 TCP flows competing for bandwidth
  ▪ Flows bottlenecked because they are sharing the same link towards Host 2
  ▪ Combined throughput cannot exceed 1000Mbps
  ▪ 3 approaches to isolate the flows’ impact on each other:
    • *Standard* switch configuration: do nothing
    • *Ingress Policing*: rate-limit traffic coming from Host 3
    • *Time Gating*: schedule the 2 flows on different time slots
The Time-Aware Scheduler works by following the guidelines in 802.1Qbv

- The 5 Egress Ports each have 8 Gates, which can be open or closed
- Each Gate has 1 Queue associated with it
- Whenever a Gate is open, packets from that Queue can be sent out the wire
- An internal clock generates ticks each 200ns
- At each tick, a new time slot can be created, where some Gates can be opened and some can be closed

- Effectively works like TDM (Time Division Multiplexing) for Ethernet
TSN Demo – Analysis: Scheduling configuration

• The user defines how many clock ticks each time slot takes
  ▪ The individual time slots are called *subschedules*

• Once the Time-Aware Scheduler goes through each time slot in a round-robin fashion, it starts over again periodically
  ▪ A complete period of *subschedules* is called a *schedule*

• On Egress Port 2 (toward Host 2), create a subschedule for VLAN PRIO 0 and one for PRIO 3
  ▪ Flow 1 is completely isolated from Flow 2
  ▪ Minimal interference, best utilization of bandwidth
TSN Software Development Kit

Q1 2017
- Consolidate TSN Programming into single application
- File based configuration
- 1588 Boundary clocking on LS1021A (2-step)

Q2 2017
- Netconf configuration of TSN ->

Q3 2017
- 1588 Transparent clocking (1-step)
Configuration using SJA1105-Tool
Configuration using NETCONF / YANG

The NETCONF protocol defines mechanism for device management and configuration retrieval and modification. It uses a remote procedure call (RPC) paradigm and a system of exposing device (server) capabilities, which enables a client to adjust to the specific features of any network equipment.

NETCONF Configuration Layers:

<table>
<thead>
<tr>
<th></th>
<th>Content</th>
<th>Configuration data</th>
<th>Notification data</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Content</td>
<td>Configuration data</td>
<td>Notification data</td>
</tr>
<tr>
<td>2</td>
<td>Operations</td>
<td>&lt;edit-config&gt;</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Messages</td>
<td>&lt;rpc&gt;, &lt;rpc-reply&gt;</td>
<td>&lt;notification&gt;</td>
</tr>
<tr>
<td>4</td>
<td>Secure</td>
<td>Transport SSH, TLS</td>
<td></td>
</tr>
</tbody>
</table>
IEEE1588 - PTPd stack support

- Full IEEE 1588-2008 (PTPv2) protocol implementation
- Software-only timestamping, advanced filtering, robust to network failures
- Multi-platform: Linux, FreeBSD, OpenBSD, NetBSD, Solaris, various embedded OS
- Support for PTP Default profile, Telecom profile (G.8265) and Enterprise profile
- IPv4 Multicast, unicast and Ethernet operation
- Highly configurable
- Advanced Leap Second handling
- Integration with NTPd as failover time source

<table>
<thead>
<tr>
<th>Board</th>
<th>Clock Type</th>
<th>Interfaces used</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>BC</td>
<td>Interface 1, Interface 2.</td>
</tr>
<tr>
<td>B</td>
<td>OC</td>
<td>Interface 1</td>
</tr>
<tr>
<td>C</td>
<td>OC</td>
<td>Interface 1</td>
</tr>
</tbody>
</table>
Coming soon - Layerscape LS1028A – Industry Ready

- Dual core ARM® 64 bit processors
- ARM® V8
- L2 Cache
- DDR
- Integrated ECC
- Trust Architecture
- GPU and LCD Controller
- GPU
- TSN Ethernet Controller
- TSN Ethernet Controller
- 4 Port TSN Ethernet Switch
- Next Generation Ethernet Controllers with TSN (TSN Endpoint)
- Integrated TSN Switch
SECURE CONNECTIONS FOR A SMARTER WORLD